06-25-03 AF/2818

Appellant	Frankie F. Roohparvar
Serial No.	09/608,580
Filing Date	June 30, 2000
Group Art Unit	2818
Examiner	Trong Q. Phan
Confirmation No.	9345
Attorney Docket No.	400.006US01

TRANSMITTAL FORM UNDER 37 CFR 1.10 (LARGE ENTITY)

Title: ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY

Commissioner for Patent
MS AF
Attn: Board of Patent Appeals and Interferences
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following documents are enclosed:
X An Appeal Brief in triplicate includes Title Page and Table of Contents (1 pg.); Brief (pgs. 2-35); Appendix I (pgs. 36-41) and Appendix II (pgs. 42-46) (46 pgs. Total))
X Copies of U.S. Pat. No. 5,263,003, 6,532,522 and 5,539,696, in triplicate
X A check in the amount of $320.00 for the Appeal Brief Fee.
X An itemized return receipt postcard.

Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.

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Express Mail" mailing label number: EV324609117US Date of Deposit: June 24, 2003
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(LARGE ENTITY TRANSMITTAL UNDER 37 C.F.R. 1.10)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	Frankie F. Roohparvar	**APPEAL BRIEF**
Serial No.	09/608,580	
Filing Date	June 30, 2000	
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Table of Contents

1. Introduction

On April 24, 2002, Appellant filed a notice of appeal from the final rejection of claims 1-27 set forth in the Final Office Action mailed January 24, 2003. Three copies of this Appeal Brief are hereby timely filed on June 24, 2003, and are accompanied by a fee in the amount of $320.00 as required under 37 C.F.R. §1.17(c).

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee Micron Technology, Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants that will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-27 are pending in the application and are the subject of this appeal. In the Final Office Action mailed January 24, 2003 claims 2, 19-20 and 22-23 were rejected under 35 U.S.C. §112, first paragraph; claims 1-13 were rejected under 35 U.S.C. §102(b) as being anticipated by Cowles et al. (U.S. Patent 5,263,003); and claims 14-27 were rejected under 35 U.S.C. §102(b) as being anticipated by Patel (U.S. Patent 5,539,696). See Appendix I for claim set.

5. Summary of the Amendments

An amendment after final has not been filed in this case.

6. Summary of the Invention

In synchronous memory systems, such as SDRAM, a latency period is typically required between a write access and a read access to the same memory device. In the synchronous memory art this minimum time is due to internal memory device resource conflicts (such as the write execution path, the read execution path, write recovery, and precharge times) that prohibit read operations from immediately following a write operation. Non-volatile memory devices, which include Flash memory device, do not have these same internal memory device resource conflicts. The present invention provides methods and apparatuses for implementing a zero latency bus turnaround in synchronous memory, and in particular, synchronous non-volatile memory (such as synchronous Flash memory), that includes providing an internal data latch to hold a write access/data and allow it to proceed internal to the memory device while a read access is received and processed on the following clock cycle. In addition, because of the internal write data latch, read-to-write latency is reduced. By utilizing the internal write latch there is no need to wait for a read command to complete internal to the synchronous memory after the read column command cycle. This allows the synchronous memory or synchronous non-volatile memory to receive the first command (the load command register (LCR) command for a synchronous Flash memory) of a write command sequence on the first clock cycle immediately following a read column command without having to wait for a column address strobe (CAS) time latency period to allow the read access to complete. *See, e.g.,* Application Page 41, Line 6 to Page 43, Line 7; and Figs. 9, 12, 30-31.

7. Issues Presented for Review

The question presented in this appeal is whether the Examiner erred in rejecting claims 2, 19-20 and 22-23 under 35 U.S.C. §112, first paragraph; rejecting claims 1-13 under 35 U.S.C. §102(b) as being anticipated by Cowles et al. (U.S. Patent 5,263,003); and rejecting claims 14-27 under 35 U.S.C. §102(b) as being anticipated by Patel (U.S. Patent 5,539,696).

8. Grouping of Claims

Claims 1-27 are grouped by independent claims 1, 6, 11, 14, 19, 22, and 24 and stand or fall on their own merit for the reasons detailed below. In addition, dependent claims 18, 21, and 27, describing synchronous non-volatile memory and depending from the independent claims 14, 19, and 24 respectively also stand on their own merit for the reasons detailed below. Each of these claims is patentably distinct, as explained herein.

9. Argument

A. Rejection of Claims 1-27 under 35 U.S.C. §112 and 102

i. The Applicable Law

35 U.S.C. § 112

The Examiner has the burden under 35 U.S.C. § 112 of "presenting evidence or reasons why persons skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. In re Wertheim, 5541 F.2d 257 at 265, 191 U.S.P.Q. 90 at 98 (CCPA 1976). (*See*, MPEP §2163.04). Further, in rejecting a claim based on an alleged lack of written description, "the examiner should: (A) identify the claim limitation not described; and (B) provide reasons why persons skilled in the art at the time the application was filed would not have recognized the description of this limitation in the disclosure of the application as filed." (*See,* MPEP §2163.04, I, § 706.03(c), and § 706.03(c), Form ¶ 7.31.02, Examiner Note, Item 3.)

Inherent elements of a claim or patent application are supported by disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage. Thus, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. See In re Reynolds, 443 F.2d 384, 170 U.S.P.Q. 94 (CCPA 1971); In re Smythe, 480 F.2d 1376, 178 U.S.P.Q. 279 (CCPA 1973). (*See,* MPEP §2163.07(a)). "To establish inherency, the extrinsic evidence 'must make

clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted). (*See,* MPEP §2163.07(a) and §2112).

35 U.S.C. §102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987); (*See,* MPEP §2131). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989); (*See,* MPEP §2131). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond,* 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990); (*See,* MPEP §2131).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.,* 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

Inherency allows for anticipation to occur even if the prior art reference relied on does not expressly disclose a minor aspect of the claimed invention, by the claim that the minor aspect was inherent. Thus, inherency permits, in very limited circumstances, an invention to be anticipated by prior art that is lacking minor, well known features in the claimed invention. "For a prior art reference to anticipate a claim, the reference must disclose each and every element of

the claim with sufficient clarity to prove its existence in the prior art. . . . Although this disclosure requirement presupposes the knowledge of one skilled in the art of the claimed invention, that presumed knowledge does not grant a license to read into the prior art reference teachings that are not there." *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 43 USPQ 2d 1481, 1490 (Fed. Cir. 1997). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted); (*See,* MPEP §2163.07(a) and §2112). Thus, in establishing inherency for an element in a recited reference there may be no other possible interpretation by a person of ordinary skill of the characteristics of that element. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original); (*See*, MPEP §2112). Extrinsic evidence may be used to explain but not expand the meaning of terms and phrases used in the reference relied upon as anticipatory of the claimed subject matter. *In re Baxter Travenol Labs*, 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991); (*See*, MPEP §2131.01, II). (*See also,* MPEP §2163.07(a), §2112, and §2112.01).

Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). (*See,* MPEP §2112.01). "When the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). (*See,* MPEP §2112.01). Therefore, the *prima facie* case can be rebutted by evidence showing that the prior art products do not necessarily possess the

characteristics of the claimed product. *In re Best*, 562 F.2d at 1255, 195 USPQ at 433. (*See*, MPEP §2112 and §2112.01.)

ii. Scope and Content of Prior Art

Two prior art references were cited by the Examiner against the claims in issue. The first reference is Cowles et al., U.S. Pat. No. 5,263,003, issued on November 16, 1993 ("Cowles et al."). Cowles et al. relates to a method and apparatus for a Flash memory system in a system controller of a (industrial) controller that utilizes a memory controller to operate and store data words in two memory banks formed from multiple non-synchronous Flash memory devices. Cowles et al. also details a system that contains a serial I/O (SIO) communication controller which services two synchronous communication channels, and a clock circuit, in addition to a system controller, and Flash memory. Cowles et al. also describes a burst addressing mode of multiple consecutive reads or multiple consecutive writes utilizing the addressing mode ability of the underlying Flash memory devices. Cowles et al. also describes storing a duplicate copy of Flash memory system operating routines (that contain the software drivers for operating the Flash memory system and the individual Flash memory devices it contains) in the unselected bank of Flash memory devices while the selected bank of Flash memory devices is erased and reprogrammed, so that they are backed up and not lost. Cowles et al. also discloses that only an entire memory bank can be reprogrammed (written) at once after it has been through an erasure cycle.

Cowles et al. does not teach or disclose single synchronous memory devices (in particular, synchronous Flash memory devices), or a write access followed immediately by a read access as disclosed in the present application.

The second reference is Patel, U.S. Pat. No. 5,539,696, issued on July 23, 1996 ("Patel"). Patel relates to a method and apparatus that allows faster burst data write operations to a memory device (DRAM, SDRAM, EEPROM, PROM, and ROM) by utilizing parallel input latches to contain multiple write accesses, each latch coupled to a single memory bank. In particular, Patel

discusses dividing the banks of a SDRAM memory array into column independent sections that are simultaneously written to from two parallel input latches. Figure 3 of Patel teaches a latch circuit 100 that contains latches 102, 104, 106, and 108 and a write latch control circuit 110 wherein the write control circuit controls which latch section is used to receive data for its coupled array bank in combination with the column address. In addition, Figure 1 of Patel teaches a digital processor 12 that is coupled to a synchronous peripheral I/O device 26 and to a SDRAM 14.

Patel does not teach or disclose, a write latch as disclosed in the present application. Patel also does not teach or discuss Flash memory devices (in particular, synchronous Flash memory devices), or a write access followed immediately by a read access as disclosed in the present application.

iii. Analysis

A. Rejections Under 35 U.S.C. § 112

Claims 2, 19-20 and 22-23 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Appellant respectfully traverses the rejection.

Appellant notes that only in the Advisory Action dated April 11, 2003 did the Examiner give guidance to the reasons for his rejection of Claims 2, 19-20 and 22-23 under 35 U.S.C. §112, first paragraph. In the Office Action dated January 24, 2003 the Examiner stated only that "[t]he features as recited in claims 2, 19-20, and 22-23 are not understood because they are not described in the specification." The Office Action gave no further explanation of which specific elements in claims 2, 19-20, and 22-23 were considered not to be described in the specification as required under MPEP § 706.03(c) and MPEP § 706.03(c), Form ¶ 7.31.02, Examiner Note, Item 3. Prior to this, in the previous Office Action Response mailed December 3, 2002, and in

the Response to Final Office Action mailed March 24, 2003, the Appellant specifically requested further clarification in response to the Examiner's previous rejection of claims 2, 19-20, and 22-23 under 35 U.S.C. § 112, first paragraph, stating, "Applicant is also unsure as to which features of claims 2, 19-20, and 22-23 that the Examiner claimed were not described in the specification." In addition to this request, in the Response to Final mailed March 24, 2003, Appellant provided citations to support in the specification of the present Application for the elements of claims 2, 19-20, and 22-23. These citations have apparently not even been considered.

Appellant also respectfully notes that the Examiner has rejected portions of the present Claims (and various portions of the Specification) under 35 USC §112 in every interaction with the Appellant. After reviewing the file history, Appellant submits that the Patent Office has apparently failed to take reasonable care in presenting its arguments and rejections. It is only after nearly two years of prosecution that the Patent Office has chosen to bring up points that Appellant respectfully submits should have brought up in one of the previous office actions, the current number of which is six. In addition, it is only now, after filing of a Notice of Appeal, that the Patent Office has chosen to even partially explain its reasoning and the specific elements of claims 2, 19-20, and 22-23 that it considers not to have support for in the current rejections under 35 USC §112. Appellant continues to respond to the items the Patent Office brings up, but respectfully requests a complete action on the merits, identifying and explaining all major issues so that the Appellant may completely address all of the Examiner's arguments under 35 USC §112 and that the Application may be moved forward in Examination.

MPEP 706 and 706.03 recite in relevant parts:

> **706 Rejection of Claims**
> After the application has been read and the claimed invention understood, a prior art search for the claimed invention is made. With the results of the prior art search, including any references provided by the applicant, the patent application should be reviewed and analyzed in conjunction with the state of the prior art to determine whether the claims define a useful, novel, non-obvious, and enabled invention that has been clearly described in the specification. ***The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity***

to provide evidence of patentability and otherwise reply completely at the earliest opportunity. The examiner then reviews all the evidence, including arguments and evidence responsive to any rejection before issuing the next Office action.

706.03 Rejections Not Based on Prior Art
The primary object of the examination of an application is to determine whether or not the claims are patentable over the prior art. This consideration should not be relegated to a secondary position while undue emphasis is given to nonprior art or "technical" rejections. ***Effort in examining should be concentrated on truly essential matters, minimizing or eliminating effort on technical rejections which are not really critical. Where a major technical rejection is proper (e.g., lack of proper disclosure, undue breadth, utility, etc.) such rejection should be stated with a full development of the reasons rather than by a mere conclusion coupled with some stereotyped expression.***

Appellant has been afforded no such courtesy. Each new Office Action maintains a rejection under 35 USC §112 and, even though several reviews of the Application have been made by the Examiner, new rejections under 35 USC §112 are still being entered in new Office Actions. Appellant hopes that the newly presented remarks and citations will result in the end of rejections of the Application under 35 USC §112 and allowance and issuance of the current claims.

Claims 1 and 2 (repeated herein for convenience)

1. A method of writing to a synchronous non-volatile memory device comprising:
receiving write data on a first clock cycle and executing a data write operation;
and
executing a data read operation on a next clock cycle immediately following the first clock cycle.

2. The method of claim 1 wherein the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

In the Advisory Action mailed April 11, 2003, the Examiner rejected Claim 2 under 35 U.S.C. §112, first paragraph, stating, "[f]or claim 2, nowhere in the specification is seen to describe the data write operation is executed on a first memory bank and the data read operation is executed on a second memory bank."

Appellant respectfully disagrees with the Examiner and traverses the rejection. Appellant submits that claim 2 is supported by its original disclosure, as well as by at least the following sections of the original specification:

Pg. 40, ln. 25-27: "Referring to Figure 30, the timing of a write operation followed by a read to a different bank is illustrated. In this operation, a write is performed to bank a and a subsequent read is performed to bank b."

Pg. 32, ln. 7-9: "Read-while-write functionality allows a background operation write or erase to be performed on any bank while simultaneously reading any other bank."

Pg. 26, ln. 4-6: "An ISM WRITE or ERASE operation to any bank can occur simultaneously to a READ operation to any other bank."

Pg. 41, ln. 6-21:

> "The synchronous Flash memory provides for a latency free write operation. This is different from a SDRAM that requires the system to provide latency for write operations, just like a read operation. So the write operation does not take away from the system bus as many cycles as the SDRAM takes, and hence can improve the system read throughput, see Figure 12 where the write data, Din, is provided on the same clock cycle as the write command and column address. The clock cycle, T1, of Figure 12 does not need to be a NOP command (see Figure 30). The read command can be provided on the next clock cycle following the write data. Thus, while the read operation requires that the DQ connections remain available for a predetermined number of clock cycles following the read command (latency), the DQ connections can be used immediately after the write command is provided (no latency). As such, the present invention allows for zero bus turn around capability. This is substantially different from the SDRAM, where multiple

waits are required on the system bus when going between read and write operations. The synchronous flash provides these two features, and could improve bus throughput."

As these sections clearly state, and Figure 30 shows, the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

Appellant submits that from above cited sections, it is clear that the application in its original form contains sufficient subject matter to support the claim limitations of claim 2, namely that the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

Claims 19 and 22 (repeated herein for convenience)

19. A method of operating a synchronous memory device comprising:

receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle; and

receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection.

22. A method of initiating a write operation in a memory system, the method comprises:

providing a read command from a processor to a synchronous memory device;

providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation;

providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection.

In the Advisory Action mailed April 11, 2003, the Examiner rejected Claims 19 and 22 under 35 U.S.C. §112, first paragraph, stating, "[f]or claims 19 and 22, nowhere in the specification is seen to describe the method of receiving a read command on a first clock cycle and receiving a write command on a second clock cycle immediately following the first clock cycle. The specification only describes receiving a write command on a first clock cycle and receiving a read command on a second clock cycle immediately following the first clock cycle in lines 19-26 of page 42."

Appellant respectfully disagrees with the Examiner and traverses this rejection. Appellant submits that receiving a read command on a first clock cycle and receiving the first command of a write command sequence on a second clock cycle immediately following the first clock cycle as recited in claims 19 and 22 is at least supported by the original claims, and also by Figure 9 and Page 42, Line 27 to Page 43, Line 7, which states:

"The present invention can also eliminate clock, or CAS, latency between read and subsequent write operations. Referring to Figure 9, the LCR command (40H) is provided on clock cycle T1 immediately following the read column cycle (T0). As explained, the write operation command sequence includes at least three clock cycles: an LCR cycle, an active/row cycle, and a write/column cycle. Depending upon the latency of the read operation, one or more NOP clock cycles may be provided to avoid bus contention. The preset invention, therefore, does not require latency between the read column command cycle and the LCR write cycle. The present invention, therefore, provides for more

efficient data bus utilization by allowing for read-to-write without latency, and write-to-read without clock cycle delays."

As Figure 9 clearly shows, and the Application from Page 42, Line 27 to Page 43, Line 7 states, the first command of the write command sequence immediately follows on a second clock cycle the read command that occurs on a first clock cycle.

Appellant submits that from above cited section and Figure, it is clear that the application in its original form contains sufficient subject matter to support the claim limitations of claims 19 and 22, namely that the first command of the write command sequence immediately follows on a second clock cycle the read command that occurs on a first clock cycle.

Claims 20 & 23 (repeated herein for convenience)

20. The method of claim 19 wherein the write command sequence comprises:
a load command register cycle used to initiate the write operation;
an active cycle used to define and activate a selected row of the memory array; and
a write cycle used to define a column of the memory array and provide write data on the external data connection.

23. The method of claim 22 wherein the write command sequence comprises:
a load command register cycle used to initiate the write operation;
an active cycle used to define and activate a selected row of the memory array; and
a write cycle used to define a column of the memory array and provide write data on the external data connection.

In the Advisory Action mailed April 11, 2003, the Examiner rejected Claims 20 and 23 under 35 U.S.C. §112, first paragraph, stating, "[f]or claims 20 and 23, nowhere in the specification is seen to describe the write command sequence comprising a load command register cycle, an active cycle and a write cycle."

Appellant respectfully disagrees with the Examiner and traverses this rejection. Appellant submits that the write command sequence comprising a load command register cycle, an active cycle and a write cycle as recited in claims 20 and 23 is supported by at least the original claim language, and by the following:

Figure 9 and Page 42, Line 28 to Page 43, Line 2:

"Referring to Figure 9, the LCR command (40H) is provided on clock cycle T1 immediately following the read column cycle (T0). As explained, the write operation command sequence includes at least three clock cycles: an LCR cycle, an active/row cycle, and a write/column cycle."

Truth Table 2 and Page 32, Lines 7-11:

"For a write operation, the LCR-ACTIVE-WRITE command sequences in Truth Table 2 must be completed on consecutive clock cycles."

Page 33, Lines 9-26:

"Three consecutive commands on consecutive clock edges are needed to input data to the array (NOPs and Command Inhibits are permitted between cycles). In the first cycle, a LOAD COMMAND REGISTER command is given with WRITE SETUP (40H) on A0-A7, and the bank address is issued on BA0, BA1. The next command is ACTIVE, which activates the row address and confirms the bank address. The third cycle is WRITE, during which the starting column, the bank address, and data are issued. The ISM status bit will be set on the following clock edge (subject to CAS latencies). While the ISM executes the WRITE, the ISM status bit (SR7) will be at 0. A READ operation to the bank under ISM control may produce invalid data. When the ISM status bit (SR7) is set to a logic 1, the WRITE has been completed, and the bank will be in the array read mode and ready for an executable command. Writing to hardware-protected blocks also requires that the RP# pin be set to VHH prior to the third cycle (WRITE), and RP# must

be held at VHH until the ISM WRITE operation is complete. The write and erase status bits (SR4 and SR5) will be set if the LCR-ACTIVE-WRITE command sequence is not completed on consecutive cycles or the bank address changes for any of the three cycles. After the ISM has initiated the WRITE, it cannot be aborted except by a RESET or by powering down the part. Doing either during a WRITE may corrupt the data being written."

As Figure 9 and Truth Table 2 clearly show, and the Application from Page 42, Line 28 to Page 43, Line 2, Page 32, Lines 7-11, and Page 33, Lines 9-26 states, the first command of the write command sequence "includes at least three clock cycles: an LCR cycle, an active/row cycle, and a write/column cycle."

Appellant submits that from above cited section and Figure, it is clear that the application in its original form contains sufficient subject matter to support the claim limitations of claims 20 and 23, namely that the write operation command sequence includes at least three clock cycles: an LCR cycle, an active/row cycle, and a write/column cycle.

Furthermore, the Appellant respectfully maintains that the elements of the claims 2, 19-20 and 22-23 are described in the specification, as the claims as originally filed are considered to be part of the disclosure. *See, e.g.,* MPEP §608.01(l)

608.01(l) Original Claims

In establishing a disclosure, applicant may rely not only on the description and drawing as filed but also on the original claims if their content justifies it.

Where subject matter not shown in the drawing or described in the description is claimed in the application as filed, and such original claim itself constitutes a clear disclosure of this subject matter, then the claim should be treated on its merits, and requirement made to amend the drawing and description to show this subject matter. The claim should not be attacked either by objection or rejection because this subject matter is lacking in the drawing and description. It is the drawing and description that are defective, not the claim.

As has been stated above, to support a rejection under § 112, the claim limitation alleged to not be described must be identified, and the Examiner must "provide reasons why persons skilled in the art at the time the application was filed would not have recognized the description of this limitation in the disclosure of the application as filed."

The Appellant submits that persons of ordinary skill in the field would have found that the Appellant was in possession of the invention at the time of the filing of the Application on the basis of the disclosure therein, specifically as outlined in the original claims and by the support above. MPEP §2163.04 places the burden on the Examiner to show and provide reasons why persons skilled in the art would not have recognized the description of the limitation in the disclosure of the application as filed, stating in part, "[a] description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption." See, e.g., *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). (*See,* MPEP §2163.04). The Examiner has attempted to point out differences between the disclosure and the claims, but the differences are not actually present. In fact, as discussed above, Appellant submits that the disclosure and claims as filed fully support claims 2, 19-20 and 22-23.

Accordingly, Appellant submits that the rejection under 35 U.S.C. 112 is improper, as the Application as originally filed includes full support for the subject matter of claims 2, 19-20, and 22-23.

Additional citations to the Application to support for elements of claims 2, 19-20, and 22-23 are also provided in Appendix II.

Appellant respectfully contends that relevant features of claims 2, 19-20, and 22-23 have been described in the specification to allow one skilled in the art to practice the invention. Therefore Appellant requests that the Examiner's rejection of claims 2, 19-20, and 22-23 under 35 U.S.C. § 112, first paragraph, be reversed.

B. Claim Rejections Under 35 U.S.C. § 102

The Appellant respectfully submits that each of the claims 1-27 contain elements or limitations not present in the cited art, and as such, the rejections discussed below under 35 U.S.C. § 102(b) are improper and not supported.

1. Claims 1-13

Claims 1-13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Cowles et al. (U.S. Patent 5,263,003). Appellant respectfully disagrees with the Examiner and traverses this rejection. Appellant submits that claims 1-13 are allowable for the following reasons.

In the Office Actions dated August 20, 2002, and January 24, 2003, the Examiner stated that Figures 1-3 of Cowles et al. detail a synchronous flash memory system, citing lines 24-27 of column 5 of Cowles et al. In these Office Actions and in the telephonic interview with the Appellant on March 19, 2003, the Examiner stated that because Cowles et al. details a system that contains a serial I/O (SIO) communication controller 44 which services two synchronous communication channels, a clock circuit 60, a system controller 61, and a Flash memory 55 that the system is inherently a synchronous non-volatile Flash memory system, regardless of the type of Flash memory that is coupled to the system.

In the Advisory Action of April 11, 2003, the Examiner stated, "Cowles et al., 5,263,003, clearly disclose 'a flash memory of a non-volatile storage device' (see line 9, column 1) and the key word 'synchronous' (see line 27, column 5). Therefore, in one way or another way, this flash memory of a non-volatile storage device must be a synchronous non-volatile device in view of the plain language such as Applicant's synchronous non-volatile memory device unless claims 1-13 further recite the specific synchronous operation for the claimed non-volatile memory device."

Appellant respectfully notes that Cowles et al. is directed to a memory controller and a flash memory system having multiple individual flash memory devices and not to an individual synchronous non-volatile memory device. Claim 1 is directed to "[a] method of writing to a synchronous non-volatile memory device." Claim 6 is directed to "[a] method of operating a synchronous memory device." And Claim 11 is directed to "[a] method of writing to a synchronous memory device." As such, the Appellant submits on the plain language of claims 1, 6, and 11 that Cowles et al. fails the all element rule for independent claims 1, 6, and 11.

The Appellant also respectfully notes that Cowles et al. does not state that its memory is synchronous Flash memory or memory of a synchronous interface type. As such, the Appellant submits that Cowles et al. fails the all element rule for independent claims 1, 6, and 11.

In addition, the Examiner stated that "[t]herefore, in one way or another way, this flash memory of a non-volatile storage device must be a synchronous non-volatile device in view of the plain language. . ." In the Office Action dated January 24, 2003, the Examiner stated in regards to Cowles et al., "therefore, it must be inherently a synchronous non-volatile flash memory system." The Appellant strongly disagrees with the assertion that a system containing a synchronous component or a system with a memory that accepts a clock signal means that the memory of the system is inherently a memory of a synchronous type and has a synchronous type of interface. Appellant respectfully submits that if the Examiner maintains that this an inherent feature, the Examiner has the burden of proving that the inherent element must of necessity only work in the manner of the Appellant's disclosed invention; if any other interpretation is possible for the inherent element relied upon the rejection cannot be maintained. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted); (*See,* MPEP §2112 and §2163.07(a)). "In relying upon the theory of inherency, the examiner

must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). (*See,* MPEP §2112).

Appellant respectfully submits that the allegedly inherent characteristic of a synchronous non-volatile memory system does not necessarily flow from the teachings of the applied prior art of Cowles et al. and would be so recognized by persons of ordinary skill. In other words, that a system containing a synchronous component or a system with a memory that accepts a clock signal necessarily implies that the memory of the system is inherently a memory of a synchronous type and has a synchronous type of interface. Appellant also submits that there are multiple possible interpretations for the fact that the memory system has a synchronous component or has a memory that accepts a clock signal besides the conclusion that the memory of the system is inherently a memory of a synchronous type and/or has a synchronous type of interface. A system is not synchronous because it is tied to a clocked processor. If so, all memory would be synchronous. One possible alternative interpretation is that the memory system of Cowles et al. interfaces to an external system that has a synchronous serial interface and therefore must have a synchronous serial interface as a component. As such, because of the fact that a person of ordinary skill in the art would not recognize that the system of Cowles et al. would necessarily be a synchronous memory system or contain a synchronous memory device, and that there are multiple possible interpretations to the system of Cowles et al. having a synchronous non-memory component or a memory that accepts a clock, the Examiner has not shown the necessity required for inherency in claiming Cowles et al. describes a synchronous non-volatile memory system or having a synchronous non-volatile memory. Therefore as Cowles et al. does not inherently describe a synchronous non-volatile memory system or having a synchronous non-volatile memory, the Appellant submits that Cowles et al. fails the all element rule for Appellant's independent claims 1, 6, and 11.

Appellant also submits that if the Patent Office maintains that Cowles et al. inherently describes a synchronous non-volatile memory system or inherently having a synchronous non-

volatile memory, that such inherency may be rebutted by the Appellant by the submission of extrinsic evidence to the contrary. A *prima facie* case of inherency by the Patent Office may be rebutted by the Appellant by an appropriate showing. "When the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). (*See,* MPEP §2112.01). In supporting or rebutting an inherent element, extrinsic evidence may be relied upon for inherent elements are considered as such in light of the ordinary person skilled in the art would know or assume. Extrinsic evidence may be used to explain but not expand the meaning of terms and phrases used in the reference relied upon as anticipatory of the claimed subject matter. *In re Baxter Travenol Labs*, 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991); (*See*, MPEP §2131.01, II).

Appellant respectfully submits that the Application utilizes the term "synchronous" in claims 1-13 of the present application to refer to a memory type that incorporates a synchronous interface. In other words, a memory of a type were the interface has a defined timing and the data is placed on or read from the memory interface at a specified time during a data access interaction with the memory. Appellant submits that such is explained in the Application as originally filed. "A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. SDRAM's can be accessed quickly, but are volatile. Many computer systems are designed to operate using SDRAM, but would benefit from non-volatile memory." *See*, Application, Page 2, Lines 11-17.

Appellant respectfully submits that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a memory device with a synchronous interface as described by Appellant above.

In addition, in support of this, Appellant, as in Appellant's Response of March 24, 2003, recites the extrinsic evidence of Barth et al. (U.S. Patent 6,532,522, Titled: "Asynchronous

request/synchronous data dynamic random access memory", Issued: March 11, 2003) to rebut the Examiner's argument of inherency and support the Appellant's claim that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a memory device with a synchronous type interface:

> In conventional memory systems, the communication between a memory controller and DRAMs is performed through asynchronous communications. For example, the memory controller uses control signals to indicate to the DRAM when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. To meet increased speed requirements, various enhanced asynchronous memory systems have been developed. One such system is the Extended Data Out (EDO) DRAM memory system.
> FIG. 1 is a block diagram illustrating a typical EDO DRAM system 100. In the EDO DRAM system 100, data transfers are performed asynchronously in response to control signals and addresses sent from pin buffers 116 of a memory controller to pin buffers 118 of the EDO DRAM over a plurality of lines 120, 122, 124, 134, and 136. Specifically, lines 122 carry an address that is stored in latches 112 and 114. Line 120 carries a row address strobe (RAS) that controls when the address stored in latch 112 is sent to row decoder 106. Line 136 carries a write enable signal that controls timing chains 108 and the direction of data flow on the bi-directional data bus 126.
> ...
> DRAMs built with an asynchronous RAS/CAS interface have difficulty meeting the high memory bandwidth demands of many current computer systems. As a result, synchronous interface standards have been proposed. These alternative interface standards include Synchronous DRAMs (SDRAMs). In contrast to the asynchronous interface of EDO DRAMS, SDRAM systems use a clock to synchronize the communication between the memory controller and the SDRAMs. Timing communication with a clock allows data to be placed on the DRAM output with more precise timing. In addition, the clock signal can be used for internal pipelining. These characteristics of synchronous communication results in higher possible transfer rates.
> FIG. 3 is a block diagram illustrating a conventional SDRAM system 300. In system 300, the memory controller includes a plurality of clocked buffers 304 and the SDRAM includes a plurality of clocked buffers 306. Data from control line 310 and an address bus 312 are received by a finite state machine 308 in the SDRAM. The output of the finite state machine 308 and the address data are sent to memory array 302 to initiate a data transfer operation.
> FIG. 4 is a timing diagram that illustrates the signals generated in system 300 during a read operation. At time T0 the memory controller places a read request on line 310 and an address on bus 312. At time T1 the SDRAM reads the information on lines 310 and 312. Between T1 and T2 the SDRAM retrieves the data located at the specified address

> from memory array 302. At time T2 the SDRAM places data from the specified address on data bus 314. At time T3 the memory controller reads the data off the data bus 314. Because system 300 is synchronous, various issues arise that do not arise in asynchronous systems. Specifically, the synchronous system has numerous pipeline stages. Unbalanced pipeline stages waste computational time. For example, if a shorter pipeline stage is fed by a longer pipeline stage, there will be some period of time in which the shorter pipeline stage remains idle after finishing its operation and before receiving the next set of data from the preceding pipeline stage. Similarly, if a short pipeline stage feeds a longer pipeline stage, the shorter pipeline stage must wait until the longer pipeline stage has completed before feeding the longer pipeline stage with new input.

See, e.g., Barth et al., column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4. Appellant further submits that the difference between asynchronous memory types (ROM, DRAM, EEPROM, Flash, and SRAM, etc.) with an asynchronous memory interface and synchronous memory types (SDRAM, DDR, etc.) with a synchronous memory interface are well known in the art. As such, Appellant submits that Barth et al. rebuts the Patent Office's assertion that Cowles et al. is inherently a system with a synchronous non-volatile Flash memory and submits that one of ordinary skill in the art would recognize Cowles et al. as describing a non-synchronous memory system.

Appellant's claim 1 is directed to a method of writing to a synchronous non-volatile memory device comprising receiving write data on a first clock cycle and executing a data write operation, and executing a data read operation on a next clock cycle immediately following the first clock cycle. As Cowles et al. does not describe a synchronous non-volatile memory device and because Cowles et al. does describe a memory system having multiple separate non-synchronous Flash memory devices Cowles et al. does not teach or disclose all elements of claim 1.

Appellant's claim 6 is directed to a method of operating a synchronous memory device comprising receiving write data on data connections, latching the write data in a write latch, releasing the data connections after the write data is latched, and performing a read operation on the synchronous memory device while the write data is transferred from the write latch to

memory cells. As Cowles et al. does not describe a synchronous memory device and because Cowles et al. does describe a memory system having multiple separate memory devices Cowles et al. does not teach or disclose all elements of claim 6.

Appellant's claim 11 is directed to a method of writing to a synchronous memory device comprising providing a write command and write data from a processor to the synchronous memory device on a first clock cycle, storing the write data in a write latch of the synchronous memory device, and performing a write operation to copy the write data from the write latch to a memory array of the synchronous memory device, and providing a read command from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation on the memory array. As Cowles et al. does not describe a synchronous memory device and because Cowles et al. does describe a memory system having multiple separate memory devices Cowles et al. does not teach or disclose all elements of claim 11.

Appellant thus respectfully submits that because of lack of inherency and description of a synchronous memory system and/or synchronous memory device Cowles et al. fails the all element test as each and every limitation of claims 1, 6, and 11 are not described, either expressly or inherently, and therefore Appellant's independent claims 1, 6 and 11 are allowable over the cited reference.

The Examiner further stated that Cowles et al. "specifically discloses that 'these control signals indicate that a read operation is occurring and **synchronize** the flash memory control 88 to other components of the system controller 16' (see lines 19-21, column 10)." (emphasis in original).

Appellant respectfully disagrees and submits that Cowles et al. describes a programmable controller 10 having a rack 12 with a system controller 16 in it (see Figure 1, and Column 3, lines 57-68). The system controller 16 having a processor section 31 that contains a Flash memory PROM 55, the Flash memory PROM 55 containing a Flash memory controller 88 (see Figures 2 and 3, Column 4, lines 44-58, Column 6, lines 22-34, Column 7, lines 39-44, and

Column 8, lines 41-45). The Appellant further submits that Cowles et al. column 10, lines 16-24 describes the Flash memory controller 88 synchronizing itself to the system controller 16 that it is a part of and does not describe synchronizing to a Flash memory device. In addition, as stated above, the Appellant submits that Cowles et al. does not state that Flash memory system is synchronous Flash memory device or system. Furthermore, Appellant submits that Cowles et al., Column 10, lines 19-21 does not teach or disclose that the read operation that is occurring is a synchronous read operation.

Appellant thus respectfully submits that Cowles et al. fails the all element test as each and every limitation of claims 1, 6, and 11 are not described, either expressly or inherently, and therefore Appellant's independent claims 1, 6 and 11 are allowable over the cited reference.

The Examiner also stated that Cowles et al. "clearly discloses that 'once one bank of the flash memory 55 has been erased, it will be reprogrammed immediately' (see lines 55-56, column 15) and 'Once a complete erasure of the memory circuit has been verified, reprogramming can commence. All the memory devices are placed simultaneously into a write state . . . **Then** the contents of the given storage location are read.' (see lines 13-18, column 3)." (emphasis in original).

Appellant respectfully disagrees and submits that the full text of Cowles et al. Column 15, lines 55-56 stating "[t]ypically, once one bank of the flash memory 55 has been erased, it will be reprogrammed immediately" does not teach or describe a write sequence followed by a read and/or a read sequence followed by a write on its plain language.

In addition, Appellant respectfully submits that Cowles et al. Column 3, lines 13-18 does not teach or describe a write sequence followed immediately by a read. Appellant notes that Cowles et al. does not state anything about the relative timing of these interactions with its Flash memory. Appellant submits that absent a disclosure of this timing or a showing that it inherently occurs without a latency period or in a synchronous manner that Cowles et al. does not anticipate the elements of Appellant's claims 1, 6, and 11. As such, Cowles et al. Column 3, lines 13-18 does not teach or describe a write sequence on a first clock cycle followed immediately by a read

cycle on a second clock cycle. In fact, Appellant submits also notes that Cowles et al. Column 3, line 18-20 does not describe executing a read operation while a write operation is transferred from a memory latch to memory cells. In addition, Appellant respectfully notes that Cowles et al. is directed to a memory controller and a flash memory system having multiple individual flash memory devices and not to an individual synchronous memory device.

In the Office Actions dated August 20, 2002 and January 24, 2003, the Examiner further stated that in Cowles et al. the write cycle immediately followed a read cycle, citing lines 40-62 of column 7. Appellant disagrees and submits that column 7, lines 40-62 describe a burst addressing mode of multiple consecutive reads or multiple consecutive writes utilizing the addressing mode ability of the underlying Flash memory devices and does not teach or disclose a write cycle immediately followed by a read cycle. Appellant also notes that Cowles et al. discloses that only an entire memory bank can be reprogrammed (written) at once after it has been through an erasure cycle. Appellant submits that this mandatory erasure cycle before writing eliminates the possibility of a write immediately following a read cycle. See e.g., Cowles et al., column 13, lines 38-50. As such, with the burst addressing mode and the mandatory erasure before reprogramming of an entire memory bank at once, the Appellant submits that Cowles et al. does not teach or disclose a write cycle immediately following a read cycle.

In addition, Appellant notes again that the memory banks 71 and 72 cited by the Examiner in Cowles et al. disclose memory banks comprised of individual Flash memory devices and as such do not occur within a single Flash memory device as disclosed by the Appellant's specification. As such, Cowles et al. does not teach or disclose an individual synchronous Flash memory device.

The Examiner further stated that, in Cowles et al., duplicate copies of data in the Flash memory 55 can be updated/latched/hold, citing lines 13-21 of column 12. Appellant disagrees and submits that column 12, lines 13-21 describe storing a duplicate copy of Flash memory system operating routines (that contain the software drivers for operating the Flash memory system and the individual Flash memory devices it contains) in the unselected bank of Flash

memory devices while the selected bank of Flash memory devices is erased and reprogrammed, so that they are backed up and not lost. Appellant submits that these are duplicate copies of data already stored in the Flash memory system and not data currently being written/read from the Flash memory system. Additionally, these are not latches but Flash memory devices, thus the data is held in the Flash memory arrays of the Flash memory devices. Also, that the elements cited by the Examiner are multiple Flash memory devices and not latches within a single Flash memory device. Further, as stated above, this functionality backs up the software driver routines for the Flash memory so that they are not lost during reprogramming. As such, with the cited elements being Flash Memory devices and not latches, the data being held having already been written/stored in the Flash memory system, and it not being an individual Flash memory device, that Cowles et al. does not teach or disclose a latch for latching write data as used and recited in Appellant's claims.

Appellant's claim 1 is directed to a method of writing to a synchronous non-volatile memory device comprising receiving write data on a first clock cycle and executing a data write operation, and executing a data read operation on a next clock cycle immediately following the first clock cycle. Cowles et al. does not describe a synchronous non-volatile memory device. Cowles et al. does describe a memory system having multiple separate non-synchronous Flash memory devices. Cowles et al. does not describe a write latch, and Cowles et al. does not describe a synchronous write interaction followed immediately on the next clock cycle by a read interaction. Therefore Cowles et al. does not teach or disclose all elements of claim 1.

Appellant's claim 6 is directed to a method of operating a synchronous memory device comprising receiving write data on data connections, latching the write data in a write latch, releasing the data connections after the write data is latched, and performing a read operation on the synchronous memory device while the write data is transferred from the write latch to memory cells. Cowles et al. does not describe a synchronous non-volatile memory device. Cowles et al. does describe a memory system having multiple separate non-synchronous Flash memory devices. Cowles et al. does not describe a write latch, and Cowles et al. does not

describe a executing a read operation while a write operation is transferred from a memory latch to memory cells. Therefore Cowles et al. does not teach or disclose all elements of claim 6.

Appellant's claim 11 is directed to a method of writing to a synchronous memory device comprising providing a write command and write data from a processor to the synchronous memory device on a first clock cycle, storing the write data in a write latch of the synchronous memory device, and performing a write operation to copy the write data from the write latch to a memory array of the synchronous memory device, and providing a read command from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation on the memory array. Cowles et al. does not describe a synchronous non-volatile memory device. Cowles et al. does describe a memory system having multiple separate non-synchronous Flash memory devices. Cowles et al. does not describe executing a read operation while a write operation is transferred from a memory latch to memory cells. Cowles et al. does not describe a write latch, and Cowles et al. does not describe a synchronous write interaction followed immediately on the next clock cycle by a read interaction. Therefore Cowles et al. does not teach or disclose all elements of claim 11.

As such, since Cowles et al. does not describe a synchronous non-volatile/Flash memory device, Cowles et al. does describe memory banks with multiple individual Flash memory devices, Cowles et al. does not describe a write cycle immediately following a read, and Cowles et al. does not teach or disclose write data latches, each and every limitation of the claims 1-13 is not present in Cowles et al., and the rejection is improper. Claims 1-13 are allowable.

Appellant respectfully contends that claims 1-13 have been shown to be patentably distinct from the cited reference. Accordingly, Appellant requests the Examiner's final rejection under 35 U.S.C. § 102(b) be reversed and requests reconsideration and allowance of claims 1-13.

2. Claims 14-27

Claims 14-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Patel (U.S. Patent 5,539,696).

Appellant respectfully traverses this rejection and requests reversal of the Examiner's Final Rejection and reconsideration of the claims. Appellant submits that claims 14-27 are allowable for the following reasons.

As the Examiner noted, Appellant's claims 14, 19, 22, and 24 recite synchronous memory devices. However, Appellant respectfully notes that claims 14, 19, and 24 have dependent claims (claims 18, 21, and 27) that focus on synchronous non-volatile memory. While this is secondary to the issue of anticipation of the synchronous memory of claims 14, 19, 22, and 24, as above, the Appellant strongly disagrees with the Examiner's assertion of Patel inherently enabling synchronous non-volatile EEPROM, PROM, or ROM devices. Patel discloses a parallel latch invention in reference to SDRAM devices, but absent a direct teaching or disclosure this does not make the recited non-volatile EEPROM, PROM, or ROM devices also synchronous and most certainly does not enable the practice of synchronous non-volatile EEPROM, PROM, or ROM devices.

Regarding the rejection of dependent claims 18, 21, and 27, Appellant submits that it is not necessarily the case that the recited non-volatile EEPROM, PROM, or ROM devices are synchronous non-volatile EEPROM, PROM, or ROM devices. It is entirely possible that the recited non-volatile EEPROM, PROM, or ROM devices are asynchronous devices that incorporate the disclosed latching system. In fact, the Appellant submits that it is highly likely to be so. As such, given the possibility of a viable alternative interpretation for Patel's recitation of non-volatile EEPROM, PROM, or ROM devices, the Examiner's assertion of inherency cannot stand. Appellant also submits that one of ordinary skill in the art would also not see Patel as describing the invention in regards to synchronous non-volatile memory or enabling the practice of synchronous non-volatile memory. Appellant further submits that the difference between

asynchronous memory types (ROM, DRAM, EEPROM, Flash, and SRAM, etc.) with an asynchronous memory interface and synchronous memory types (SDRAM, DDR, etc.) is well known in the art. As inherency is interpreted in light of how one skilled in the art would interpret the recited element, the Examiner's assertion of Patel disclosing synchronous non-volatile memory cannot be supported or maintained.

Appellant further rebuts this argument of inherency by noting the above recited reference of Barth et al. In addition, Appellant notes that the present Application's own background states," Computers almost always contain a small amount of read-only memory (ROM) that holds instructions for starting up the computer. Unlike RAM, ROM cannot be written to. An EEPROM (electrically erasable programmable read-only memory) is a special type non-volatile ROM that can be erased by exposing it to an electrical charge. Like other types of ROM, EEPROM is traditionally not as fast as RAM. EEPROM comprise a large number of memory cells having electrically isolated gates (floating gates). Data is stored in the memory cells in the form of charge on the floating gates. Charge is transported to or removed from the floating gates by programming and erase operations, respectively. Yet another type of non-volatile memory is a Flash memory. A Flash memory is a type of EEPROM that can be erased and reprogrammed in blocks instead of one byte at a time." (Application, Page 1, Lines 18-28)

As such, the Examiner's assertion of inherent synchronous non-volatile memory as an element of Patel is improper and the rejection of claims 18, 21, and 27 fails the all element rule. Appellant respectfully requests reversal of the Examiner's rejection and reconsideration of claims 18, 21, and 27.

Regarding to the larger issue of the anticipation of the Appellant's independent claims 14, 19, 22, and 24, Appellant submits that Patel teaches a synchronous memory device that allows faster burst data write operations by using parallel latches of the input buffers, where the parallel latches are directly coupled to a single memory bank, see column 5, line 64 to column 6, line 26. The banks of the memory array are divided into column independent sections that are simultaneously written to from the buffer parallel latches.

The Examiner stated that Patel disclosed a synchronous memory that included write latches 110 and 102, 104, 106, and 108, as shown in Figure 3. The Examiner further stated that synchronous memory cell array 14 and write latches 102-110 are coupled to the input/output data buffer circuit I/O 26 of Figure 1.

Appellant disagrees and submits that Figure 3 of Patel teaches a latch circuit 100 that contains latches 102, 104, 106, and 108 and a write latch control circuit 110 wherein the write control circuit which latch to receive data for its coupled array bank in combination with the column address and does not teach or disclose a write latch where the write latch may be coupled to any memory bank. *See, e.g.,* Patel, column 11, lines 31-38.

In addition, Appellant also disagrees with the Examiner and submits that Patel does not teach or suggest a system having a synchronous memory wherein the synchronous memory has an input/output data buffer for bi-directional data communication with an external device coupled to a write data latch, as asserted by the Examiner by reference to the separate synchronous peripheral I/O device 26 of Figure 1. Appellant submits that Figure 1 of Patel teaches a separate synchronous peripheral I/O device 26 that is not internal to the synchronous memory device which is coupled to a digital processor 12 and a input/output data buffer circuit I/O of a synchronous memory device. *See, e.g.,* Patel, column 4, lines 31-37.

Appellant also submits that the presence of synchronous dynamic memory devices that can be written or read in a burst mode does not preempt the present invention absent a disclosure of the claimed feature or an argument that the feature is inherently disclosed and necessarily the case. There is no discussion in Patel of the timing between write and read operations. It is also well known in the synchronous dynamic memory art that there is a minimum time (such as write recovery and precharge times) that prohibit read operations from immediately following a write operation, and therefore Patel cannot support an inherency argument. Thus Patel neither directly or inherently discloses a write operation followed immediately by a read operation or a reduced latency read followed by a write as described in the present disclosure and claimed in claims 14-27.

Appellant's claim 14 is directed to a synchronous memory device comprising a memory array arranged in rows and columns, data communication connections for bi-directional data communication with an external device, data buffer coupled to the data communication connections to manage the bi-directional data communication, and a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections. As Patel does not describe does not teach or disclose a data buffer coupled to the data communication connections to manage the bi-directional data communications, a write latch where the write latch may be coupled to any memory bank, but teaches multiple write latches where each write latch is directly connected to a single memory bank, and there is no discussion in Patel of the timing between write and read operations, Patel does not teach or disclose all elements of claim 14.

Appellant's claim 19 is directed to a method of operating a synchronous memory device comprising receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle, and receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection. As Patel does not describe does not teach or disclose a write following a read, and there is no discussion in Patel of the timing between write and read operations, Patel does not teach or disclose all elements of claim 19.

Appellant's claim 22 is directed to a method of initiating a write operation in a memory system, the method comprises providing a read command from a processor to a synchronous memory device, providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation, and providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle

to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection. As Patel does not describe does not teach or disclose a write following a read, and there is no discussion in Patel of the timing between write and read operations, Patel does not teach or disclose all elements of claim 22.

Appellant's claim 24 is directed to a memory system comprising a processor, and a synchronous memory device coupled to the processor via a bi-directional data bus, the synchronous memory device comprises a memory array arranged in rows and columns, data communication connections coupled to the bi-directional data bus, an input/output data buffer coupled to the data communication connections to manage bi-directional data communication, and a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections. As Patel does not describe does not teach or disclose a write latch where the write latch may be coupled to any memory bank, but teaches multiple write latches where each write latch is directly connected to a single memory bank, and the cited I/O buffer 26 is not internal to the memory device, Patel does not teach or disclose all elements of claim 24.

As such, since Patel does not describe a synchronous memory device with write latches which may be coupled to any memory bank, the cited I/O buffer 26 is not internal to the memory device, and that a write following a read is not disclosed, or disclose a synchronous non-volatile/Flash memory device, that each and every limitation of the claims 14-27 are not present in Patel, and the rejection is improper. Claims 14-27 are allowable.

Appellant respectfully contends that claims 14-27 have been shown to be patentably distinct from the cited reference. Accordingly, Appellant requests reversal of the Examiner's Final Rejection under 35 U.S.C. § 102(b) and reconsideration and allowance of claims 14-27.

iv. The Dependent Claims Are Also Allowable

As claims 2-5, 7-10, 12-13, 15-18, 20-21, 23, and 25-27 depend from and further define patentable claims 1, 6, 11, 14, 19, 22, and 24, they are also considered to be in condition for allowance.

v. Seasonable Challenge

As the Appellant's challenge to the Examiner's rejections has occurred within the time period set by statute, it is considered to be seasonable.

10. Summary

Appellant has set forth reasons why the Examiner is incorrect in maintaining his rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of non-enablement of claims 2, 19-20, and 22-23 as shown in the cited references from the Application.

The Examiner has also failed to set forth a prima facie case of inherency of the reference Cowles et al. in regards to teaching a synchronous memory device. Cowles et al. does not necessarily lead to a conclusion that its disclosed memory devices are synchronous or have a synchronous interface or that one of ordinary skill in the art would have concluded it was such. The Examiner has also failed to set forth a prima facie case of inherency of the reference Patel in regards to teaching a synchronous non-volatile memory device; discussion of the invention of Patel in regards to SDRAM does not necessarily lead to a conclusion that in practicing the invention with other memory devices such as SRAM, EEPROM, PROM, and ROM, that these memory devices are synchronous or have a synchronous interface or that one of ordinary skill in the art would have concluded it was such.

Further, the cited references of Cowles et al. and Patel do not teach or suggest all the claim limitations of Appellant's claims 1-27.

In regards to claims 1-13, rejected in view of Cowles et al. under 35 USC §102(b); as Cowles et al. does not describe a synchronous non-volatile/Flash memory device, Cowles et al. does describe memory banks with multiple individual Flash memory devices, Cowles et al. does not describe a write cycle immediately following a read, and Cowles et al. does not teach or disclose write data latches, each and every limitation of the claims 1-13 are not present in Cowles et al., and the rejection is improper. Therefore claims 1-13 are allowable.

In regards to claims 14-27, rejected in view of Patel under 35 USC §102(b); as Patel does not describe a synchronous memory device with write latches which may be coupled to any memory bank, in Patel the cited I/O buffer 26 is not internal to the memory device, in Patel a write following a read is not disclosed, and Patel does not disclose a synchronous non-volatile/Flash memory device, that each and every limitation of the claims 14-27 are not present in Patel, and the rejection is improper. Therefore claims 14-27 are allowable.

Appellant respectfully submits that, for the above reasons, claims 1-27 are allowable over the cited art. Therefore, reversal of the Examiner's rejections and allowance of the claims is respectfully requested.

Respectfully submitted,

Date: 6/24/03

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Appendix I

Claims on Appeal

1. (original) A method of writing to a synchronous non-volatile memory device comprising:
receiving write data on a first clock cycle and executing a data write operation; and
executing a data read operation on a next clock cycle immediately following the first clock cycle.

2. (original) The method of claim 1 wherein the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

3. (original) The method of claim 1 further comprising latching the write data on the first clock cycle.

4. (original) The method of claim 1 wherein executing the data write operation comprises:
receiving a write command;
receiving a row address; and
receiving a column address, wherein the column address is received on the first clock cycle in synchronization with the write data.

5. (original) The method of claim 1 further comprises:
latching the write data in a write latch on the first clock cycle; and
performing a write operation during the next clock cycle to store the write data in the synchronous non-volatile memory device.

6. (original) A method of operating a synchronous memory device comprising:

receiving write data on data connections;

latching the write data in a write latch;

releasing the data connections after the write data is latched; and

performing a read operation on the synchronous memory device while the write data is transferred from the write latch to memory cells.

7. (original) The method of claim 6 wherein the read operation is initiated in response to a read command received by the synchronous memory device on a second clock cycle immediately following a first clock cycle coincident with receiving the write data.

8. (previously amended) The method of claim 6 further comprises:

receiving a row address on a first clock cycle;

receiving a column address on a second clock cycle following the first clock cycle, wherein the write data is received on the data connections on the second clock cycle.

9. (original) The method of claim 8 wherein the read operation is initiated in response to a read command received by the synchronous memory device on a third clock cycle immediately following a second clock cycle.

10. (original) The method of claim 6 wherein the synchronous memory device comprises an array of non-volatile memory cells.

11. (original) A method of writing to a synchronous memory device comprising:

providing a write command and write data from a processor to the synchronous memory device on a first clock cycle;

storing the write data in a write latch of the synchronous memory device; and

performing a write operation to copy the write data from the write latch to a memory array of the synchronous memory device; and

providing a read command from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation on the memory array.

12. (original) The method of claim 11 wherein the write data is copied to a first bank of the memory array and the read operation is performed on a second bank of the memory array.

13. (original) The method of claim 11 wherein the processor provides a row address, and a column address, wherein the column address is provided on the first clock cycle in synchronization with the write data.

14. (original) A synchronous memory device comprising:

a memory array arranged in rows and columns;

data communication connections for bi-directional data communication with an external device;

data buffer coupled to the data communication connections to manage the bi-directional data communication; and

a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

15. (original) The synchronous memory device of claim 14 further comprising control circuitry to copy the data from the write latch to the memory array.

16. (previously amended) The synchronous memory device of claim 15 wherein the memory array is arranged in a plurality of memory blocks, and the control circuitry is configured to copy the data from the write latch to a first block of the plurality of memory blocks.

17. (original) The synchronous memory device of claim 16 wherein the control circuitry is further configured to read data from a second block of the plurality of memory blocks while the data is copied to the first block.

18. (original) The synchronous memory device of claim 14 wherein the memory array comprises non-volatile memory cells.

19. (original) A method of operating a synchronous memory device comprising:

receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle; and

receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection.

20. (original) The method of claim 19 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

21. (original) The method of claim 19 wherein the memory array comprises non-volatile memory cells.

22. (original) A method of initiating a write operation in a memory system, the method comprises:

providing a read command from a processor to a synchronous memory device;

providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation;

providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection..

23. (original) The method of claim 22 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

24. (original) A memory system comprising:

a processor; and

a synchronous memory device coupled to the processor via a bi-directional data bus, the synchronous memory device comprises,

a memory array arranged in rows and columns;

data communication connections coupled to the bi-directional data bus;

an input/output data buffer coupled to the data communication connections to manage bi-directional data communication; and

a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

25. (previously amended) The memory system of claim 24 wherein the memory array is arranged in a plurality of memory blocks, and the synchronous memory comprises control circuitry

configured to copy the data from the write latch to a first block of the plurality of memory blocks.

26. (original) The memory system of claim 25 wherein the control circuitry is further configured to read data from a second block of the plurality of memory blocks while the data is copied to the first block.

27. (original) The memory system of claim 24 wherein the memory array comprises non-volatile memory cells.

Appendix II

Supplemental support for Claims 2, 19-20, and 22-23 under 35 U.S.C. §112, first paragraph

In the Advisory Action mailed April 11, 2003, the Examiner rejected Claims 2, 19-20, and 22-23 under 35 U.S.C. §112, first paragraph.

Specifically, the elements of claims 2, 19-20, and 22-23 are additionally supported in the description by at least the following {Claims 1-2, 19-20, and 22-23 are repeated herein for convenience of reference}:

Claim 2

1. A method of writing to a synchronous non-volatile memory device comprising: receiving write data on a first clock cycle and executing a data write operation; and executing a data read operation on a next clock cycle immediately following the first clock cycle.

2. The method of claim 1 wherein the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

Element (Support)

data write operation -- Pg. 16, ln. 18 to Pg. 20, ln. 16; Pg. 24, ln. 1-3; Pg. 32, ln. 3-13; and Pg. 33, ln. 9-26.

executed -- Pg. 6, ln. 14-29; Pg. 16, ln. 18 to Pg. 20, ln. 16; Pg. 24, ln. 1-3; and Pg. 33, ln. 9-26.

first memory bank -- Pg. 32, ln. 3-13; Pg. 40, ln. 25 to Pg. 41, ln. 4; and Fig. 30

synchronous non-volatile memory device -- Pg. 6, ln. 14-29; and Pg. 41, ln. 6-21.

data read operation -- Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 24, ln. 1-3.

executed -- Pg. 6, ln. 14-29; Pg. 16, ln. 18 to Pg. 20, ln. 16; Pg. 24, ln. 1-3; and Pg. 33, ln. 9-26.

second memory bank -- Pg. 32, ln. 3-13; Pg. 40, ln. 25 to Pg. 41, ln. 4; and Fig. 30.

General support citations for Claim 2 – Pg. 25, ln. 27 to Pg. 26, ln. 10; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 40, ln. 25 to Pg. 41, ln. 4; Fig. 30; Fig. 31; Pg. 41, ln. 6-21; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

Claims 19 & 20

19. A method of operating a synchronous memory device comprising:
receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle; and
receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection.

20. The method of claim 19 wherein the write command sequence comprises:
a load command register cycle used to initiate the write operation;
an active cycle used to define and activate a selected row of the memory array; and
a write cycle used to define a column of the memory array and provide write data on the external data connection.

Element (Support)

Claim 19 –

synchronous memory device -- Pg. 2, ln. 11-21

receiving a read command and corresponding column address on a first clock cycle -- Pg. 16, ln. 18 to Pg. 20, ln. 16

to request output data from a memory array wherein the output data is provided on an external data connection -- Pg. 16, ln. 18 to Pg. 20, ln. 16

a predefined number of clock cycles following the first clock cycle -- Pg. 16, ln. 18 to Pg. 20, ln. 16

receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle -- Pg. 16, ln. 18 to Pg. 20, ln. 16; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Fig. 9.

to initiate a write operation to the memory array -- Pg. 16, ln. 18 to Pg. 20, ln. 16

such that the write command is provided in coincidence with or prior to providing the output data on the external data connection -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 32, ln. 3-13; and Pg. 25, ln. 27 to Pg. 26, ln. 10.

Claim 20 –

write command sequence -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; and Truth Table 2.

a load command register cycle used to initiate the write operation -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 33, ln. 9-26.

an active cycle used to define and activate a selected row of the memory array -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 33, ln. 9-26.

a write cycle used to define a column of the memory array and provide write data on the external data connection -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 33, ln. 9-26.

General support citations for Claim 19 – Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 25, ln. 27 to Pg. 26, ln. 10; Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 2, ln. 11-21.

General support citations for Claim 20 – Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Truth Table 2; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

Claims 22-23

22. A method of initiating a write operation in a memory system, the method comprises:
providing a read command from a processor to a synchronous memory device;
providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation;
providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection.

23. The method of claim 22 wherein the write command sequence comprises:
a load command register cycle used to initiate the write operation;
an active cycle used to define and activate a selected row of the memory array; and
a write cycle used to define a column of the memory array and provide write data on the external data connection.

Element (Support)

Claim 22 –

initiating a write operation in a memory system -- Pg. 42, ln. 19 to Pg. 43, ln. 7; and Fig. 9

providing a read command from a processor to a synchronous memory device -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; and Pg. 16, ln. 18 to Pg. 20, ln. 16

providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation -- Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; and Pg. 16, ln. 18 to Pg. 20, ln. 16

providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle -- Pg. 32, ln. 3-13; Truth Table 2; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Fig. 9

to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection -- Pg. 42, ln. 19 to Pg. 43, ln. 7; and Fig. 9

Claim 23 –

wherein the write command sequence comprises -- Pg. 32, ln. 3-13

a load command register cycle used to initiate the write operation -- Pg. 33, ln. 9-26

an active cycle used to define and activate a selected row of the memory array -- Pg. 33, ln. 9-26;

a write cycle used to define a column of the memory array and provide write data on the external data connection -- Pg. 33, ln. 9-26;

General support citations for Claim 22 – Pg. 32, ln. 3-13; Fig. 9; Truth Table 2; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

General support citations for Claim 23 – Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Truth Table 2.